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10/717,335	11/19/2003	Joichi Bita	3408.68745	8257

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EXAMINER	
DILLON, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,335	BITA ET AL.	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-29-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/717335 has a total of 16 claims pending in the application, there are 2 independent claims and 14 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

II. STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

3. As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on an application filed in November 22, 2002.

III. INFORMATION CONCERNING DRAWINGS

4. The applicant's drawings submitted November 19, 2003 are acceptable for examination purposes.

IV. ACKNOWLEDGEMENT OF INFORMATION DISCLOSURE STATEMENT

5. The information disclosure statement (IDS) submitted on March 29, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

6. As required by M.P.E.P. ' 609 (C), the applicant's submission of the Information Disclosure Statement dated March 29, 2004 is acknowledged by the

examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. ' 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

V. OBJECTIONS TO THE APPLICATION

7. **Claims 1-16** are objected to because of the following informalities:

a. **Claim 1** recites the phrasing "to data access request" on page 23 line 4. The objection would be withdrawn if it were amended to read "to a data access request".

b. **Claim 9** recites the elements "a pair of controller" on page 26 lines 5-6. The objection would be withdrawn if it were amended to read "a pair of controllers".

c. **Claims 2-8 and 11-16** are objected to by virtue of their dependency.

Appropriate correction is required.

VI. REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC ' 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. **Claims 1-16** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. **Claim 1** recites the element "the mirror area of said first cache memory" (page 23 lines 15-16). There is insufficient antecedent basis for this claim. The Examiner notes that this objection would be withdrawn if the claim were amended to read "a mirror area of said first cache memory", and for the purposes of further examination will read it as such.

11. **Claim 1** recites the limitation "the write data" on page 23 line 22. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether "a data write request" as cited on lines 17-18 inherently contains "write data". The Examiner notes that this rejection would be withdrawn if the claim on lines 17-18 were amended to read "and wherein when said first controller received a data write request **containing write data** from said requesting apparatus", and for the purposes of further examination will read it as such.

12. **Claim 2** recites the limitation "said first and second controllers mutually notify the sizes of said first and second cache memories" on page 24 lines 2-3. It is unclear what the two controllers notify, what the notification is and when the notification occurs. The Examiner notes that this rejection would be withdrawn if page 24 lines 2-5 were amended to read "said first and second controllers allocate the mirror areas of said first and second cache memories according to the sizes of said first and second cache memories", and for the purposes of further examination will read it as such.

13. **Claim 4** recites the limitation "the storage apparatus" on page 24 line 16. There if insufficient antecedent basis for this limitation in the claim. It is unclear whether this limitation intends to refer to the storage control apparatus or the

storage device, both cited on page 23 lines 3-4. The Examiner notes that this rejection would be withdrawn if page 24 line 16 was amended to read "the storage device", and for the purposes of further examination will read it as such.

14. **Claim 4** recites the limitation "the copy page" on page 24 line 17. There is insufficient antecedent basis for this limitation in the claim. It is unclear whether the limitation refers to "a storage page" as cited on page 23 line 20 or is attempting to introduce a distinct element. The Examiner notes that this rejection would be withdrawn if page 24 line 17 was amended to read "the storage page", and for the purposes of further examination will read it as such.

15. **Claim 6** recites the limitation "the write data" on page 25 line 5. There is insufficient antecedent basis for this limitation in the claim. The Examiner notes that this rejection is related to the rejection of Claim 1 above regarding the limitation "the write data" on page 23 line 22, and that if the above rejection is amended as desired then this rejection will be withdrawn.

16. **Claim 8** recites the limitations "said control unit" and "said node channel circuit" on page 25 line 22. There is insufficient antecedent basis for this limitation in the claim. As per claim 7, the applicant discloses a first and second controller each comprising a control unit, and it is unclear which control unit the limitation "said control unit" refers to. The Examiner notes that this rejection would be withdrawn if the claim on line 22 was amended to read "said first control unit" and "said first node channel circuit", and for the purposes of further examination will be read as such.

17. **Claim 9** recites the limitation "the mirror area" on page 26 line 11. There is insufficient antecedent basis for this limitation in the claim. The rejection rational and withdrawal conditions are analogous to the rejection of Claim 1 above regarding the element "the mirror area of said first cache memory" (page 23 lines 15-16).

18. **Claim 10** recites the limitation "mutually notifying the sizes of said first and second cache memories between both controllers" on page 26 lines 21-22. It is unclear what the two controllers notify, what the notification is and when the notification occurs. The Examiner notes that this rejection would be withdrawn if page 24 lines 21-24 were amended to read "allocating the mirror areas of said first and second cache memories according to the sizes of said first and second cache memories", and for the purposes of further examination will read it as such.

19. **Claims 3, 5, 7 and 11-16** are rejected by virtue of their dependency.

VII. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 103 – Hubis and Kitamura

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claims 1-2, 4, 7, 9-10, 12 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* in view of Kitamura et al. *(US Patent Number 6,247,012)*.

22. As per **Claim 1**, Hubis discloses a storage control apparatus *(figure 1)* for accessing a storage device *(shared storage devices 108)* according to data access request *(host write command 128, column 3 lines 49-50)* from a requesting apparatus *(host computer 1, figure 1)*, comprising:

a first controller *(RAID controller 1, figure 1)* which has a first cache memory *(cache 112-1, figure 1)* and is in charge *(via bus 110, figure 1, see below)* of a first storage device *(any of shared storage devices 108)* out of a plurality of storage devices *(shared storage devices 108)*; and

a second controller *(RAID controller 2)* which has a second cache memory *(cache 112-2, figure 1)* and is in charge *(via bus 110, figure 1, see below)* of a second storage device *(any of shared storage devices 108)* out of said plurality of storage devices, and

a mirror area *(write mirror cache 118-2, figure 2)* of said second cache memory, and a mirror area *(write mirror cache 118-1, figure 2)* of said first cache memory,

and wherein when said first controller received a data write request *(host write command 128, column 3 lines 49-50)* from said requesting apparatus, said first controller allocates a page *(destination in first controller, see below)* in a read/write area *(write cache 116-1, figure 2)* of said first cache memory, acquires a storage page *(subset of mirror area, see below)* in the mirror area of said

second cache memory, writes *(transfer 107-1, figure 2)* the write data *(write data 138, column 3 line 51)* from said requesting apparatus to the page allocated in the read/write area of said first cache memory, and copies *(column 3 lines 55-58)* the write data to the acquired page in the mirror area of said second cache memory.

The Examiner notes that inherent in writing data to the read/write area in the first controller is the data being written to a subset of the read/write area, where a subset is either the entirety or a part of the read/write area. Subsequently, this subset fulfills the limitation "a page in a read/write area" cited on page 23 line 19. It is also inherent in copying the data to the mirror area of the second controller that the data is written to a subset of the mirror area, and this subset fulfills the limitation "a storage page in the mirror area" cited on page 23 line 20.

Hubis does not expressly disclose said first controller further comprising a first mirror management table for managing the mirror area of said second cache memory, and said second controller further comprising a second mirror management table for managing the mirror area of said first cache memory.

Kitamura discloses a mirror management table *(mirror management table 35, figure 12)* for managing a mirror area *(back-up copy of the primary data, column 2 lines 37-38)* of a memory (*secondary data storage system, column 2 lines 36-37*).

Hubis and Kitamura are analogous art in that they both deal with managing the mirroring of data in distinct locations.

At the time of the invention it would have been obvious to a person ordinary skill in the art to use Kitamura's mirror management table to manage the cache mirroring taught by Hubis .

The motivation for doing so would have been the ease of managing the storage locations in the memory's mirror. Kitamura discloses that mirror management permits the system to register content items to be mirrored, mirroring conditions and the storage location of an archive *(column 14 lines 21-25)*.

Therefore, it would have been obvious to combine Kitamura's mirror management table with the cache mirroring of Hubis for the benefit of managing storage locations to obtain the invention as specified in claim 1.

23. As per **Claim 2**, Hubis and Kitamura disclose the storage control apparatus according to claim 1, wherein said first and second controllers mutually notify the sizes of said first and second cache memories *(see below)*, allocate the mirror areas of said first and second cache memories according to said sizes *(see below)*, and create said first and second mirror management tables *(Kitamura, column 14 lines 20-25)*.

The concept of mirroring of a region of memory inherently involves recreating all contents of the region, including size. As per the interpretation made in paragraph 12 of this office action, the allocation of the mirror areas according to the sizes of the cache memories is then inherent in the device taught by Hubis *(Hubis, figure 2)*.

24. As per **Claim 4**, Hubis and Kitamura disclose the storage control apparatus according to claim 1, wherein when said first controller is degraded *(Hubis, "failure of controller", column 1 lines 38-41)*, said second controller takes charge of the storage apparatus which said first controller is in charge of *(Hubis, column 1 lines 45-48)*, and links the copy page in the mirror area of said second cache memory to said read/write area *(Hubis, column 1 lines 45-48)*.

25. As per **Claim 7**, Hubis discloses the storage control apparatus according to claim 1, wherein each one of said first and second controllers comprises:

a control unit *(Hubis, processor 200, figure 3)* for controlling said cache memory and said storage device; and

a node channel circuit *(Hubis, backend disk bus 110, figure 3)* for performing communication between said controllers.

26. As per **Claim 9**, Hubis discloses a storage control method for accessing a storage device *(Hubis, shared storage devices 108)* according to a data access request *(Hubis, host write command 128, column 3 lines 49-50)* from a requesting apparatus *(Hubis, host computer 1, figure 1)*, comprising the steps of:

allocating a page *(Hubis, subset of read/write area, see rejection of claim 1)* in a read/write area *(Hubis, write cache 116-1, figure 2)* of a first cache memory *(Hubis, cache 112-1, figure 1)* disposed in one controller *(Hubis, RAID controller 1, figure 1)* of a pair of controller *(Hubis, RAID controllers 1 and 2, figure 1)* when said one controller receives a data write request *(Hubis, host write command 128, column 3 lines 49-50)* from said requesting apparatus;

acquiring a storage page *(Hubis, subset of mirror area, see rejection of claim 1)* in a mirror area *(Hubis, write mirror cache 118-2, figure 2)* of a second cache memory *(Hubis, cache 112-2, figure 1)* referring to a first mirror management table *(Kitamura, mirror management table 35, figure 12)* which is disposed in said one controller for managing the mirror area of said second cache memory of said other controller;

writing *(Hubis, transfer 107-1, figure 2)* write data *(Hubis, write data 138, column 3 line 51)* from said requesting apparatus to the page allocated in the read/write area of said first cache memory; and

copying *(Hubis, column 3 lines 55-58)* the write data to the acquired page in the mirror area of said second cache memory after said writing.

27. As per **Claim 10**, Hubis and Kitamura disclose the storage control method according to claim 9, further comprising the steps of: mutually notifying the sizes of said first and second cache memories between both controllers *(see below)*; allocating the mirror areas of said first and second cache memories according to said sizes *(see below)*; and creating said first and second mirror management tables *(Kitamura, column 14 lines 20-25)*.

The concept of mirroring of a region of memory inherently involves recreating all contents of the region, including size. As per the interpretation made in paragraph 18 of this office action, the allocation of the mirror areas according to the sizes of the cache memories is then inherent in the device taught by Hubis *(Hubis, figure 2)*.

28. As per **Claim 12**, Hubis discloses the storage control method according to claim 9, further comprising a step of taking charge *(Hubis, column 1 lines 45-48)* of the storage device which said one controller is in charge of by said other controller when said one controller is degraded *(Hubis, "failure of controller", column 1 lines 38-41)*, and linking the copy page in the mirror area of said second cache memory to the read/write area of the second cache memory *(Hubis, column 1 lines 45-48)*.

29. As per **Claim 15**, Hubis discloses the storage control method according to claim 9, wherein each one of said pair of controllers comprises

a control unit *(Hubis, processor 200, figure 3)* for controlling said cache memory and said storage apparatus, and

a node channel circuit *(Hubis, backend disk bus 110, figure 3)* for performing communication between said controllers.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Tam

30. **Claims 3 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and Kitamura et al. *(US Patent Number 6,247,012)* as applied to claims 1 and 9 respectively above, in further view of Tam et al. *("A Taxonomy-Based Comparison of Several Distributed Shared Memory Systems")*.

31. As per **Claim 3**, Hubis and Kitamura disclose the storage control apparatus according to claim 1, wherein said first controller writes *(Hubis, column 3 lines 50-51)* back the data, which is written in the page allocated in the

read/write area of said first cache memory *(Hubis, column 3 lines 50-52)*, to said storage device.

Hubis and Kitamura do not disclose the storage control apparatus then releasing said acquired page of said first mirror management table.

Tam discloses releasing *("pass back the page", section 2.1.3, lines 8-9)* said acquired page *(page, section 2 paragraph 3 line 1)* of said first mirror management table.

Hubis, Kitamura and Tam are analogous art in that they deal with maintaining coherency in shared memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have the write procedure between caches of Hubis and Kitamura lock the pages they access, as per the teachings of Tam.

The motivation for doing so would have been making sure the caches are synchronized, something Hubis is concerned with *(column 1 lines 49-51)*. Tam discloses that a cache coherence protocol is needed to ensure that caches always read a valid copy of a page *(section 1.2, line 11-12)*.

Therefore, it would have been obvious to combine Hubis and Kitamura's caches with Tam's cache coherence protocol for the benefit of ensuring caches always read valid copies of pages to obtain the invention as specified in claim 3.

32. As per **Claim 11**, Hubis, Kitamura and Tam disclose the storage control method according to claim 9, further comprising the steps of:

writing back *(Hubis, column 3 lines 50-51)* the data, which is written in the page allocated in the read/write area of said first cache memory *(Hubis, column 3 lines 50-52)*, to said storage device; and

releasing *(Tam, "pass back the page", section 2.1.3, lines 8-9)* said acquired page *(Tam, page, section 2 paragraph 3 line 1)* of said first mirror management table when said write back completes.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Beardsley

33. **Claims 5 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and Kitamura et al. *(US Patent Number 6,247,012)* as applied to claims 4 and 12 respectively above, in further view of Beardsley et al. *(US Patent Number 6,304,980)*.

34. As per **Claim 5**, Hubis and Kitamura disclose the storage control apparatus according to claim 4. Hubis and Kitamura do not disclose wherein said second controller disables read/write processing to the mirror area of said second cache memory.

Beardsley discloses said second controller disabling *(step 945, figure 9)* read/write processing to the mirror area of said second cache memory.

The primary controller in Hubis accesses *(column 1 lines 37-38)* the mirror area of the second controller on the basis of write operations issued by a host *(host 102, column 1 line 17)*. Beardsley discloses issuing a stop command to host applications to stop input/output to the primary device *(step 945, figure 9)*, which effectively stops processing by the primary controller.

Hubis, Kitamura and Beardsley are analogous art in that they deal with storage controllers maintaining access to data during controller failures.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Hubis and Kitamura's secondary controller to issue a stop command to applications communicating with the primary controller in the case of a failure, as taught by Beardsley.

Beardsley teaches that the motivation for doing so would have been to maintain data integrity during several types of primary and secondary subsystem errors *(column 8, lines 39-41)*.

Therefore, it would have been obvious to combine Hubis' controllers with Beardsley's application stop command for the benefit of maintaining data integrity to obtain the invention as specified in claim 5.

35. As per **Claim 13**, Hubis, Kitamura and Beardsley disclose the storage control method according to claim 12, further comprising a step of disabling *(Beardsley, step 945, figure 9)* read/write processing to the mirror area of said second cache memory.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Rowson

36. **Claims 6 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and Kitamura et al. *(US Patent Number 6,,247,012)* as applied to claim 1 and 9 respectively above, in further view of Rowson *("Interface-Based Design")*.

37. As per **Claim 6**, Hubis and Kitamura disclose the storage control apparatus according to claim 1, wherein when said first controller received a data write request for a page from said requesting apparatus, said first controller allocates a page in the read/write area of said first cache memory, acquires a storage page in the mirror area of said second cache memory referring to said first mirror management table, writes the write data from said requesting apparatus to the allocated page in the read/write area of said first cache memory, and copies the write data to the acquired page in the mirror area of said second cache memory.

Hubis and Kitamura do not disclose the page instead being a plurality of pages, and writing the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying.

Rowson discloses a data write request for a plurality of pages *(write-burst, section 5 paragraph 6 lines 1-3)*, and writing the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying *(section 5, paragraph 7 lines 1-4)*.

Hubis, Kitamura and Rowson are analogous art in that they deal with caching write data.

It would have been obvious at the time of the invention to design Hubis' cache system to handle write bursts and cache the write data while forwarding the write command to the drive, as taught by Rowson.

The motivation for doing so, as taught by Rowson, would be to minimize on-drive resources *(section 5, paragraph 6, line 3)* and to allow the drive to read

data in an order optimized for disk scheduling *(section 5, paragraph 7, lines 10-12)*.

Therefore, it would have been obvious to combine Hubis and Kitamura's cache system with Rowson's write burst for the benefit of minimizing on drive resources and optimizing disk scheduling to obtain the invention as specified in claim 6.

38. As per **Claim 14**, Hubis, Kitamura and Rowson disclose the storage control method according to claim 9, further comprising a step of writing *(section 5, paragraph 7 lines 1-4)* the data of the next page to the next page allocated in the read/write area of said first cache memory during said copying when said one controller receives a data write request for a plurality of pages *(write-burst, section 5 paragraph 6 lines 1-3)* from said requesting apparatus.

Claim Rejections - 35 USC ' 103 – Hubis, Kitamura and Li

39. **Claims 8 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hubis *(US Patent Number 6,321,298)* and Kitamura *(US Patent Number 6,247,012)* as applied to claims 7 and 15 respectively above, in further view of Li et al *("Evaluation of Memory System Extensions")*.

40. As per **Claim 8**, Hubis and Kitamura disclose the storage control apparatus according to claim 7, wherein said control unit instructs *(Hubis, mirror cache write command, column 3 lines 57-58)* said node channel circuit to execute the transfer of data of the page allocated in the read/write area of said

first cache memory to the acquired page in the mirror area of said second cache memory, and performs said copying *(Hubis, column 3 lines 52-55)*.

Hubis and Kitamura do not disclose the transfer being a DMA transfer.

Li discloses transferring data blocks between memories where the transfer is a DMA transfer *(lines 7-17, paragraph 3 of page 91)*.

Hubis, Kitamura and Li are analogous art in that they deal with transferring data between memory elements.

It would have been obvious to one with ordinary skill in the art to utilize DMA transfer when transferring data between the first and second controllers. The motivation for doing so would have been to allow the controller's control unit to do other useful work during the period of transfer *(lines 13-14, paragraph 3 of page 91)*.

Therefore, it would have been obvious to combine the transfer of data used in Hubis and Kitamura with the DMA transfer described by Li for the benefit of increased processing time to obtain the invention as specified in claim 8.

41. As per **Claim 16**, Hubis, Kitamura and Li disclose the storage control method according to claim 15, wherein said copying step comprises a step of instructing *(Hubis, mirror cache write command, column 3 lines 57-58)* said node channel circuit to execute the DMA transfer *(Li, lines 7-17, paragraph 3 of page 91)* of the data of the page allocated in the read/write area of said first cache memory to the acquired page in the mirror area of said second cache memory and performing said copying *(Hubis, column 3 lines 52-55)*.

VIII. RELEVANT ART CITED BY THE EXAMINER

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

DeKoning et al. *(US Patent Numbers 5,761,705 and 6,567,889)* discloses maintaining cache consistency in redundant controllers for a disk drive array.

Yamamoto et al. *(US Patent Number 6,408,370)* discloses a set of controllers caching write data.

Yanai et al. *(US Patent Number 6,173,377)* discloses a remote controller mirroring data from a local controller.

Sicola et al. *(US Patent Number 5,974,506)* discloses enabling multiple cache modes in a dual cache system.

Kern et al. *(US Patent Number 5,870,537)* discloses a pair of controllers that can switch based on storage controller and device errors.

Boyle *(US Patent Number 5,864,854)* discloses maintaining a shared cache lookup table.

Arnott et al. *(US Patent Number 5,712,970)* discloses a method of reliably storing data to be written to storage using more than one controller.

Candelaria et al. *(US Patent Number 5,682,513)* discloses a data storage system providing disaster recovery by transmitting record updates to a secondary site.

IX. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

43. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(4). CLAIMS REJECTED IN THE APPLICATION

44. Per the instant office action, claims 1-16 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571-272-8010. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

IMPORTANT NOTE

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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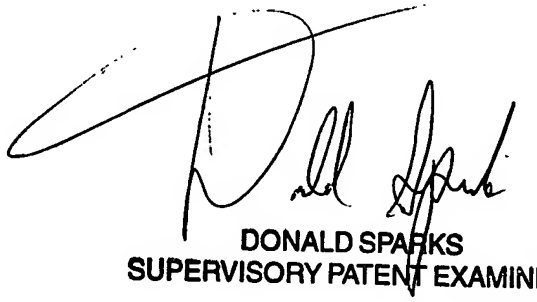

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

Sam Dillon
Examiner
Art Unit 2185